BM1385

Bitcoin Hash ASIC Datasheet

Bitmain Technologies Limited

Contents

Revision History

Revision Number	Author	Date	Description
1.0	Zhan	2015.6.16	Initial
2.0	Zhan	2015.6.30	Delete LDO_VSS

1Overview

This is a kind of high performance and low power consumption bitcoin mining ASIC.

1.1 Features

- Typical hash rate and power

Voltage(V)	Hash Rate(GH/S)	Current(A)	Total power(W)	W/GH
0.71	38.75	14.350	10.189	0.263
0.66	32.50	10.760	7.102	0.219
0.60	21.25	6.410	3.846	0.181

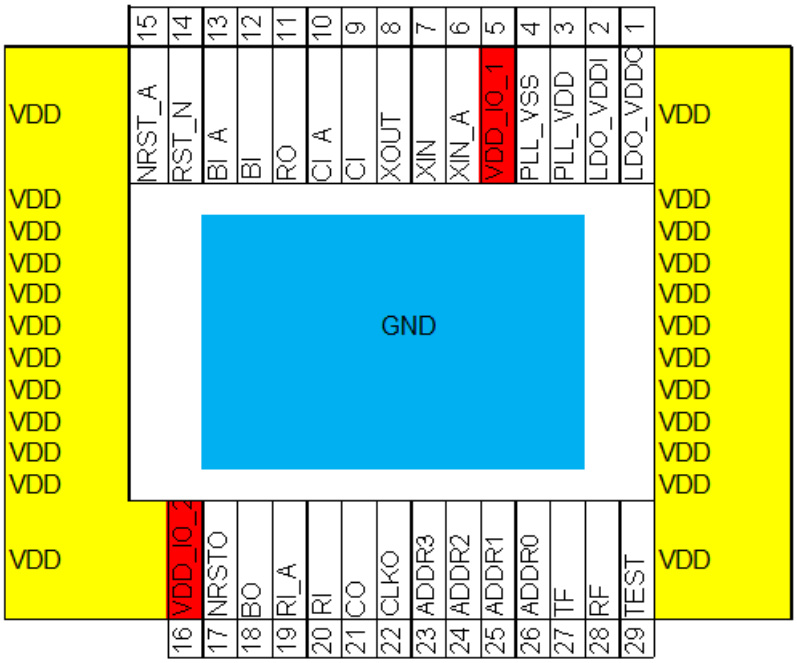
- Customized package
- Support UART communication interface
- Support chain mode, Max 256 chips per chain

1.2 Applications

- Bitcoin mining

2Pin Description

2.1 Pin Diagram



Top view

2.2 Signal Description

Name	I/O	Active Level	Description
XIN	I	N/A	Oscillator input
XOUT	O	N/A	Oscillator output
RST_N	I	L	Reset signal
TEST	I	N/A	Internal pull down. 0: Normal mode 1: Test mode
CLKOUT	O	N/A	Clock output
NRSTO	O	L	Reset output
CI	I	N/A	Command Input. Schmitt input.
CO	O	N/A	Command Output
RI	I	N/A	Respond Input. Schmitt input and internal pullup.
RO	O	N/A	Respond Output

Name	I/O	Active Level	Description
BI	I	H	Respond Busy Input. Schmit input and internal pulldown.
BO	O	H	Respond Busy Output
ADDR[3:0]			Address Input. Internal pullup.
RF	O		RO open drain output; Command Rx Flag
TF	O		Respond Tx Flag
PLL_VDD			PLL power (0.9V)
PLL_VSS			PLL ground
LDO_VDD1			LDO power input. Typical 1.8V
LDO_VDDO			LDO power output 0.9V. 1uF external capacitor.
NRST_A			Reset input. Trigger level is (-VDD，VDDPST-VDD)
BI_A			BI input. Trigger level is (-VDD，VDDPST-VDD)
CI_A			CI input. Trigger level is (-VDD，VDDPST-VDD)
XIN_A			XIN input. Trigger level is (-VDD，VDDPST-VDD)
RI_A			RI input. Trigger level is (VDD, VDDPST+VDD)

3UART description

3.1 UART protocol

The default baud rate is 115200 when the XIN clock frequency is 25MHz. it can be set via command.
Minimum RX guard time: 1 bit
TX guard time: 2 bit
RX IDLE: 16 bits
Bit order: LSB

3.2 Work format

Byte0~31 (32bytes)	Byte32~35 (4bytes)	Byte36~39 (4bytes)	Byte40~43 (4bytes)	Byte44~47 (4bytes)	Byte48~50 (3bytes)	Byte51		Byte52~63 (12bytes)
Midstate	Ignore	TM	HCN	SNO	Ignore	Bit[7]	Bit[6:0]	Data2
						Ignore	WC	

SNO: Start Nonce Offset.
WC: Work Count. It is used to index the input works.
HCN: Hash counting number. When HCN is reached, the hash core will stop hashing.
TM: Ticket Mask. It is used to set the difficulty of return nonce.

3.3 Work timing

PLLDiv1	PLLDiv2	FBDIV[11:0]	REFDIV[5:0]	POSTDIV1[2:0]	POSTDIV2[2:0]	Freq(Mhz)	step(Mhz)
0x20040	0x420	32	2	4	1	100.00	0.00
0x28040	0x420	40	s2	4	1	125.00	25.00
0x30040	0x420	48	2	4	1	150.00	25.00
0x38040	0x420	56	2	4	1	175.00	25.00
0x40040	0x420	64	2	4	1	200.00	25.00
0x48040	0x420	72	2	4	1	225.00	25.00
0x50040	0x420	80	2	4	1	250.00	25.00
0x58040	0x420	88	2	4	1	275.00	25.00
0x60040	0x420	96	2	4	1	300.00	25.00
0x68040	0x420	104	2	4	1	325.00	25.00

0x70040	0x420	112	2	4	1	350.00	25.00
0x78040	0x420	120	2	4	1	375.00	25.00
0x80040	0x420	128	2	4	1	400.00	25.00
0x61040	0x320	97	2	3	1	404.17	4.17
0x41040	0x220	65	2	2	1	406.25	2.08
0x62040	0x320	98	2	3	1	408.33	2.08
0x42040	0x220	66	2	2	1	412.50	4.17
0x63040	0x320	99	2	3	1	412.50	4.17
0x64040	0x320	100	2	3	1	416.67	4.17
0x43040	0x220	67	2	2	1	418.75	2.08
0x65040	0x320	101	2	3	1	420.83	2.08
0x44040	0x220	68	2	2	1	425.00	4.17
0x66040	0x320	102	2	3	1	425.00	4.17
0x67040	0x320	103	2	3	1	429.17	4.17
0x45040	0x220	69	2	2	1	431.25	2.08
0x68040	0x320	104	2	3	1	433.33	2.08
0x46040	0x220	70	2	2	1	437.50	4.17
0x69040	0x320	105	2	3	1	437.50	4.17
0x6a040	0x320	106	2	3	1	441.67	4.17
0x47040	0x220	71	2	2	1	443.75	2.08
0x6b040	0x320	107	2	3	1	445.83	2.08
0x48040	0x220	72	2	2	1	450.00	4.17
0x6c040	0x320	108	2	3	1	450.00	4.17
0x6d040	0x320	109	2	3	1	454.17	4.17
0x49040	0x220	73	2	2	1	456.25	2.08
0x6e040	0x320	110	2	3	1	458.33	2.08
0x4a040	0x220	74	2	2	1	462.50	4.17
0x6f040	0x320	111	2	3	1	462.50	4.17
0x70040	0x320	112	2	3	1	466.67	4.17
0x4b040	0x220	75	2	2	1	468.75	2.08
0x71040	0x320	113	2	3	1	470.83	2.08
0x4c040	0x220	76	2	2	1	475.00	4.17
0x72040	0x320	114	2	3	1	475.00	4.17
0x73040	0x320	115	2	3	1	479.17	4.17
0x4d040	0x220	77	2	2	1	481.25	2.08
0x74040	0x320	116	2	3	1	483.33	2.08
0x4e040	0x220	78	2	2	1	487.50	4.17
0x75040	0x320	117	2	3	1	487.50	4.17
0x76040	0x320	118	2	3	1	491.67	4.17
0x4f040	0x220	79	2	2	1	493.75	2.08
0x77040	0x320	119	2	3	1	495.83	2.08
0x50040	0x220	80	2	2	1	500.00	4.17
0x78040	0x320	120	2	3	1	500.00	4.17

0x79040	0x320	121	2	3	1	504.17	4.17
0x51040	0x220	81	2	2	1	506.25	2.08
0x7a040	0x320	122	2	3	1	508.33	2.08
0x52040	0x220	82	2	2	1	512.50	4.17
0x7b040	0x320	123	2	3	1	512.50	4.17
0x7c040	0x320	124	2	3	1	516.67	4.17
0x53040	0x220	83	2	2	1	518.75	2.08
0x7d040	0x320	125	2	3	1	520.83	2.08
0x54040	0x220	84	2	2	1	525.00	4.17
0x7e040	0x320	126	2	3	1	525.00	4.17
0x7f040	0x320	127	2	3	1	529.17	4.17
0x55040	0x220	85	2	2	1	531.25	2.08
0x80040	0x320	128	2	3	1	533.33	2.08
0x56040	0x220	86	2	2	1	537.50	4.17
0x57040	0x220	87	2	2	1	543.75	6.25
0x58040	0x220	88	2	2	1	550.00	6.25
0x59040	0x220	89	2	2	1	556.25	6.25
0x5a040	0x220	90	2	2	1	562.50	6.25
0x5b040	0x220	91	2	2	1	568.75	6.25
0x5c040	0x220	92	2	2	1	575.00	6.25
0x5d040	0x220	93	2	2	1	581.25	6.25
0x5e040	0x220	94	2	2	1	587.50	6.25
0x5f040	0x220	95	2	2	1	593.75	6.25
0x60040	0x220	96	2	2	1	600.00	6.25
0x61040	0x220	97	2	2	1	606.25	6.25
0x62040	0x220	98	2	2	1	612.50	6.25
0x63040	0x220	99	2	2	1	618.75	6.25
0x64040	0x220	100	2	2	1	625.00	6.25
0x65040	0x220	101	2	2	1	631.25	6.25
0x66040	0x220	102	2	2	1	637.50	6.25
0x67040	0x220	103	2	2	1	643.75	6.25
0x68040	0x220	104	2	2	1	650.00	6.25
0x69040	0x220	105	2	2	1	656.25	6.25
0x6a040	0x220	106	2	2	1	662.50	6.25
0x6b040	0x220	107	2	2	1	668.75	6.25
0x6c040	0x220	108	2	2	1	675.00	6.25
0x6d040	0x220	109	2	2	1	681.25	6.25
0x6e040	0x220	110	2	2	1	687.50	6.25
0x6f040	0x220	111	2	2	1	693.75	6.25
0x70040	0x220	112	2	2	1	700.00	6.25
0x71040	0x220	113	2	2	1	706.25	6.25
0x72040	0x220	114	2	2	1	712.50	6.25
0x73040	0x220	115	2	2	1	718.75	6.25

0x74040	0x220	116	2	2	1	725.00	6.25
0x75040	0x220	117	2	2	1	731.25	6.25
0x76040	0x220	118	2	2	1	737.50	6.25
0x77040	0x220	119	2	2	1	743.75	6.25
0x78040	0x220	120	2	2	1	750.00	6.25
0x79040	0x220	121	2	2	1	756.25	6.25
0x7a040	0x220	122	2	2	1	762.50	6.25
0x7b040	0x220	123	2	2	1	768.75	6.25
0x7c040	0x220	124	2	2	1	775.00	6.25
0x7d040	0x220	125	2	2	1	781.25	6.25
0x7e040	0x220	126	2	2	1	787.50	6.25
0x7f040	0x220	127	2	2	1	793.75	6.25
0x80040	0x220	128	2	2	1	800.00	6.25
0x41040	0x120	65	2	1	1	812.50	12.50
0x42040	0x120	66	2	1	1	825.00	12.50
0x43040	0x120	67	2	1	1	837.50	12.50
0x44040	0x120	68	2	1	1	850.00	12.50
0x45040	0x120	69	2	1	1	862.50	12.50
0x46040	0x120	70	2	1	1	875.00	12.50
0x47040	0x120	71	2	1	1	887.50	12.50
0x48040	0x120	72	2	1	1	900.00	12.50
0x49040	0x120	73	2	1	1	912.50	12.50
0x4a040	0x120	74	2	1	1	925.00	12.50
0x4b040	0x120	75	2	1	1	937.50	12.50
0x4c040	0x120	76	2	1	1	950.00	12.50
0x4d040	0x120	77	2	1	1	962.50	12.50
0x4e040	0x120	78	2	1	1	975.00	12.50
0x4f040	0x120	79	2	1	1	987.50	12.50
0x50040	0x120	80	2	1	1	1000.00	12.50

3.4 Nonce respond format

4bytes	Bit[7]	Bit[6:0]
Nonce	1	WorkCount

3.5 Configuration description

Support two modes:

- FIL (Fixed Input Length)
- VIL (Variable Input Length)

When system reset (RST_N is low), if ADDR3 is HIGH, it is FIL mode; else it is VIL mode.

3.5.1 Command

ALL	CMD[6:0]	command
0/1	1	SetAddress
1	2	SetPLLDivider2
0/1	4	GetStatus
1	5	ChainInactive
0/1	6	SetBaudOPS
1	0x7	SetPLLDivider1
0/1	0x8	SetConfig. Only valid in VIL mode.

3.5.2 SetAddress

FIL:

31	30:24	23:16	15:8	7:6	[5:0]
ALL	CMD	ADDR	Reserved	Reserved	CRC5

VIL:

Byte0			Byte1	Byte2	Byte3	Byte4	
7:5	4	3:0	7:0	7:0	7:0	7:5	4:0
TYPE=2	ALL=0	CMD	Length=5	ADDR	Reserved	Reserved	CRC5

3.5.3 ChainInactive

FIL:

31	30:24	23:16	15:8	7:5	4:0
ALL	CMD	Reserved	Reserved	Reserved	CRC5

VIL:

Byte0			Byte1	Byte2	Byte3	Byte4	
7:5	4	3:0	7:0	7:0	7:0	7:5	4:0
TYPE=2	ALL=1	CMD	Length=5	Reserved	Reserved	Reserved	CRC5

3.5.4 SetPLLDivider

SetPLLDivider1：

31	30:24	23	23:12	11	10:5	4:0

Reserved	CMD	Reserved	FBDIV[11:0]	Reserved	REFDIV[5:0]	CRC5

SetPLLDivider2：

31	30:24	23:16	15:12	10:8	7:5	4:0
ALL	CMD	ADDR	Reserved	POSTDIV1[2:0]	POSTDIV2[2:0]	CRC5

FBDIV: PLL feedback divider, range from 60 to 160.
REFDIV: PLL reference clock divider, range from 1 to 63.
POSTDIV1：PLL post divide 1, range 1 to 7.
POSTDIV2：PLL post divide 2, range 1 to 7. Total post divide is POSTDIV1* POSTDIV2.
The value of POSTDIV1 should ALWAYS be greater than or equal to POSTDIV2.

- $FOUTVCO = FREF/REFDIV \times FBDIV$
- $FOUTPOSTDIV = (FREF/REFDIV) \times FBDIV/POSTDIV1/POSTDIV2$

3.5.5 GetStatus

31	30:24	23:16	15:8	7:5	4:0
ALL	CMD	ADDR	REGADDR	Reserved	CRC5

Register Respond format:

4bytes	Bit[7:5]	Bit[4:0]
Read data of register	000	CRC5

3.5.6 SetConfig

Only valid in VIL mode.

Byte0			Byte1	Byte2	Byte3	Byte4~7	Byte8	
7:5	4	3:0	7:0	7:0	7:0		7:5	4:0
TYPE=2	ALL	CMD	Length=9	ADDR	REGADDR	REGDATA	Reserved	CRC5

4Electrical Character

4.1 Absolute Maximum Rating

Symbol	Parameter	Max value	Unit
VDD	Core Voltage	1.2	V
VCC	IO Voltage	1.98	V
PLL_DVDD	PLL Digital power	1.2	V
PLL_AVDD	PLL analog Power	1.92	V
T_{STG}	Storage Temperature	-65~150	℃

4.2 Recommended Operation Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDD	Core Voltage	0.60	0.66	0.8	V
IO_VDD	IO Voltage	1.62	1.8	1.98	V
PLL_VDD	PLL Digital power	0.81	0.9	0.99	V
T_{OPT}	Operation Temperature	0	25	125	℃

4.3 DC Characters

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage	-0.3		0.63	V
V_{IH}	Input High Voltage	1.17		1.98	V
V_{OL}	Output Low Voltage			0.45	V
V_{OH}	Output High Voltage	1.35			V
I_L	Input Leakage Current			±10	uA
V_T	I/O threshold point	0.81	0.89	0.97	V
V_{T+}	Schmitt input low to high threshold pint	0.95	1.03	1.10	V
V_{T-}	Schmitt input high to low threshold pint	0.64	0.75	0.86	V
R_{PU}	I/O internal pull-up resistor	47K	69K	106K	Ω
R_{PD}	I/O internal pull-down resistor	49K	85K	159K	Ω
I_{CC}(VCC)	Supply current of VCC		10		mA
I_{CC}(PLL)	Supply current of PLL_DVDD and PLL_AVDD		4		mA
CB_{IN}	Input pin capacitance		10		pF

CB_{OUT}	Output pin capacitance		10		pF